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SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY: PUTTUR
(AUTONOMOUS)**B. Tech II Year II Semester Supplementary Examinations February 2022****LINEAR & DIGITAL IC APPLICATIONS**

(Electronics and Communication Engineering)

Time: 3 hours

Max. Marks: 60

(Answer all Five Units 5 x 12 = 60 Marks)

UNIT-I

- 1 a Derive the expression for Inverting amplifier and draw its input and output wave forms. **6M**
b Derive the output expression for the practical integrator circuit **6M**

OR

- 2 a Draw and explain the three open loop op-amp configurations with neat circuit diagram **6M**
b Explain about the operation of sample and hold circuit with relevant waveforms. **6M**

UNIT-II

- 3 a Design the first order high pass filter and discuss its frequency response **6M**
b What is the principle operation of RC phase shift oscillator? Explain its operation. **6M**

OR

- 4 a Explain the functional block diagram of 555 timer **6M**
b Design Wien bridge oscillator using op-amp and explain its operation. **6M**

UNIT-III

- 5 a Draw and Explain about the Monolithic IC 565 **6M**
b Explain about counter type ADC with neat block diagram. **6M**

OR

- 6 a Draw and Explain about the Monolithic IC 565 **6M**
b Discuss about low voltage CMOS and Interfacing. **6M**

UNIT-IV

- 7 a Explain the various data types supported by VHDL along with examples. **6M**
b Design the logic circuit and write VHDL program for the following function. **6M**
 $F(Y) = \Pi A, B, C, D (1, 4, 5, 7, 9, 11, 12, 13, 15).$

OR

- 8 a Write a VHDL entity and Architecture for the following function. **6M**
 $F(x) = (a + b) (c.d)$ Also draw the relevant logic diagram.
b Explain in detail different modeling styles of VHDL with suitable examples. **6M**

UNIT-V

- 9 a Design a 4 to 16 decoder with 74×138 IC's. **6M**
b Design a priority encoder that can handle 32 requests. Use 74×148 and required discrete gates. Provide the truth table and explain the operation. **6M**

OR

- 10 a Design an 8-bit serial in and parallel out shift register. **6M**
b Design a 16-bit comparator using 74×85 ICs. **6M**

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